What is claimed is:

1. A method for fabricating a semiconductor device, comprising the steps of:

forming a plurality of conductive patterns on a substrate;

forming an etch stop layer along the plurality of the conductive patterns;

forming an insulation layer on an entire surface of the substrate structure;

etching selectively the insulation layer to form a plurality of contact holes exposing a portion of the etch stop layer allocated in between the conductive patterns;

forming an attack barrier layer for preventing the insulation layer from being attacked by a chemical used in a wet cleaning/etching process along a profile containing the contact hole;

forming a capping layer having an over-hang structure on an upper part of each conductive pattern;

extending an opening portion of each contact hole by performing a wet cleaning/etching process to a bottom side of each contact hole;

removing selectively a portion of the etch stop layer and the attack barrier layer disposed at the bottom side of each contact hole to expose a surface of the substrate; and

forming a plug contacted to the exposed surface of the contact hole.

2. The method as recited in claim 1, wherein the attack barrier layer is a nitride-based layer.

3. The method as recited in claim 2, wherein the attack barrier layer has a thickness ranging from about 10 Å to about 100 Å.

4. The method as recited in claim 2, wherein the wet cleaning/etching process uses a buffered oxide etchant containing ammonium hydroxide (NH_4OH) and hydrofluoric acid (HF) mixed in a ratio of about 50:1 to about 500:1 or a diluted HF solution diluted with H_2O in a ratio of about 50:1 to about 500:1.

5. The method as recited in claim 1, wherein the capping layer is made of plasma enhanced tetra-ethyl-ortho silicate (PETEOS) or undoped silicate glass (USG).

6. The method as recited in claim 1, further comprising the step of weakening bonding forces between atoms contained in sidewalls of the capping layer with use of an inert gas after forming the capping layer and wherein the sidewalls of the capping layer containing the atoms with weakened bonding forces are removed at the step of performing the wet cleaning/etching process.

7. The method as recited in claim 6, wherein the step

of weakening bonding forces between atoms contained in sidewalls of the capping layer is performed by using a plasma etching technique employing the inert gas.

8. The method as recited in claim 6, wherein, at the step of weakening bonding forces between atoms contained in sidewalls of the capping layer, the inert gas is ion-implanted onto the sidewalls of the capping layer.

9. The method as recited in claim 5, wherein the capping layer has a thickness ranging from about 500 Å to about 2000 Å.

10. The method as recited in claim 1, wherein the conductive pattern includes a gate electrode pattern, a bit line pattern or a metal wire pattern.

11. The method as recited in claim 1, wherein the plug is formed with a polysilicon layer or a tungsten layer.

12. A method for fabricating a semiconductor device, comprising the steps of:

forming a plurality of conductive patterns on a substrate;

forming an etch stop layer along the plurality of the conductive patterns;

forming an insulation layer on an entire surface of the

substrate structure;

etching selectively the insulation layer to form a plurality of contact holes exposing a portion of the etch stop layer allocated in between the conductive patterns;

forming a capping layer having an over-hang structure on an upper part of each conductive pattern;

weakening bonding forces between atoms contained in sidewalls of the capping layer with use of an inert gas;

extending an opening portion of the contact hole by performing a wet cleaning/etching process and simultaneously removing the sidewalls of the capping layer;

removing selectively a portion of the etch stop layer disposed at a bottom side of each contact hole to expose a surface of the substrate; and

forming a plug contacted to the exposed surface of the substrate.

13. The method as recited in claim 12, wherein the step of weakening bonding forces between atoms contained in sidewalls of the capping layer is performed by using a plasma etching technique employing the inert gas.

14. The method as recited in claim 12, wherein, at the step of weakening bonding forces between atoms contained in sidewalls of the capping layer, the inert gas is ion-implanted onto the sidewalls of the capping layer.

15. The method as recited in claim 12, wherein, at the step of performing a wet cleaning/etching process, the wet cleaning/etching process uses a buffered oxide etchant containing NH_4OH and HF mixed in a ratio of about 50:1 to about 500:1 or a diluted HF solution diluted with H_2O in a ratio of about 50:1 to about 500:1.

16. The method as recited in claim 12, wherein the capping layer is made of PETEOS or USG.

17. The method as recited in claim 12, wherein the conductive pattern includes a gate electrode pattern, a bit line pattern or a metal wire pattern.

18. The method as recited in claim 12, wherein the plug is made of a polysilicon layer or a tungsten layer.